TRANSMITTAL OF APPEAL BRIEF	Docket No. 20136-00305-US

In re Application of: Roy C. (deceased), Flaker et al.

Application No.	Filing Date	Examiner	Group Art Unit
09/588,351-Conf. #8116	June 7, 2000	J. A. Fenty	2815

Invention: CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Supplemental Appeal Brief in this application, with respect to the Notice of Appeal
filed: June 18, 2004 .

The fee for filing this Appeal Brief is _____ .

[X] Large Entity [ ] Small Entity

[ ] A petition for extension of time is also enclosed.

The fee for the extension of time is _____ .

[ ] A check in the amount of _____ is enclosed.

[X] Charge the amount of the fee to Deposit Account No. 22-0185 .
This sheet is submitted in duplicate.

[ ] Payment by credit card. Form PTO-2038 is attached.

[X] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 22-0185 .
This sheet is submitted in duplicate.

Dated: 3/30/05

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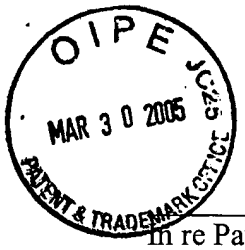

Docket No.: 20136-00305-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Roy C. (deceased), Flaker et al.

Application No.: 09/588,351 Confirmation No.: 8116

Filed: June 7, 2000 Art Unit: 2815

For: CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES Examiner: J. A. Fenty

REQUEST FOR REINSTATEMENT OF THE APPEAL AND SUPPLEMENTAL APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The undersigned requests reinstatement of the appeal in connection with the above-identified patent application. A Supplemental Brief follows addressing the issues raised in the Office Action mailed November 30, 2004. Any fee required with respect to a Petition for Extension of Time for filing this Brief, and fees therefore are dealt with in the Transmittal of the Appeal Brief document.

The Brief is transmitted in triplicate.

The following items required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206, are identical to those in the main Brief and are not repeated herein:

This Brief will supplement items VI, VIII and IX of the Brief filed on August 18, 2004.

VI. Issues

The issues on Appeal are as follows:

Are claims 6, 8, 9, 11 and 14 properly rejected under 35 U.S.C. § 102(e) as being anticipated by Okumura et al. (U.S. Pat. No. 5,892,260), and are claims 7, 10, 12 and 13 properly rejected under 35 U.S.C. § 103 as being unpatentable over Okumura et al. in view of Ohmi (U.S. Pat. No. 4,907,053)?

VIII. Arguments

The Rejection under 35 U.S.C. § 102

The rejection under 35 U.S.C. § 102(e) is identical to the rejection issued in the previous Final Rejection, and that argued in the previously submitted Brief on Appeal. The following additional comments are directed to the specific allegations of the Office Action dated November 30, 2004. The following comments address additional matters raised in the Office Action concerning this rejection.

The Office Action of November 30, 2004, on page 3 thereof characterizes the Okumura et al. reference as follows:

> Provide a pulse discharge circuit (312, 2103) connected to the at least one SOI device using the pulse discharge circuit to discharge any accumulated potential on a body of the at least one SOI device prior to accessing the at least one SOI device (col. 6, lines 28-37, col. 11, lines 50-67).

The cited passages of the reference disclose a voltage bias circuit 312 shown in the figures. The bias circuit establishes a "standby mode" which increases the threshold voltage for an FET by applying a bias voltage to a back gate of the FET. Col. 11, lines 50-67, and col. 12, lines 1-19.

From the description in col. 12, lines 20-26, and with reference to FIGS. 22A-22E, it appears that the V substrate voltage is grounded. When the device is switched from standby to active, the back gate voltage is increased. Claims 6, 9, 11 and 14 all refer specifically to removing charge on a substrate by connecting the substrate to ground prior to accessing the device. It is not seen where this reference suggests removing charge from the substrate. The reference is directed to changing the threshold voltage of a device, and not for removing accumulated charge prior to access to speed-up operation.

Further, the Office Action indicates that the following elements are shown in Okumura et al.: a delay element (capacitor) coupled to the input signal, an output signal coupled to the input signal of the output signal driving the circuit.

It is submitted that these elements cannot be found in the cited reference.

In reviewing the reference, the principle concept of generating a pulse, for discharging accumulating charge prior to reading a device does not appear to be disclosed.

The Rejection under 35 U.S.C. § 103

The Office Action of November 30, 2004, cites a new reference to Ohmi (U.S. Pat. No. 4,907,053) which allegedly in combination with Okumura et al. renders the subject matter of claims 7, 10, 12 and 13 unpatentable. Allegedly lines 33-35 of Ohmi discloses using a pulse circuit. In referring to this portion of the reference, a description is provided regarding the channel length versus the potential barrier height. It is submitted that there is nothing in this portion of the reference which refers to any pulse circuit or pulse applied to discharge accumulated charge. The references is directed to a particular type of insulated gate transistor which serves as a driving transistor, without any reference to discharging accumulative charge prior to accessing the device.

IX. SUMMARY

It is requested that the Honorable Board of Patent Appeals and Interferences consider the above remarks when deciding the present Appeal.

Dated: 3/30/05

Respectfully submitted,

By _____

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